REMARKS

Reconsideration and withdrawal of the rejections of the application are respectfully requested in view of the foregoing amendments and following remarks.

I. STATUS OF THE CLAIMS AND FORMAL MATTERS

The Office Action indicates that claims 1-5 and 14-16 and 26 are pending in this application. By this amendment, independent claims 1 and 14 are amended for additional clarity. No new matter has been added. It is submitted that the claims, as originally presented, were in full compliance with the requirements of 35 U.S.C. §112. Changes to claims are not made for the purpose of patentability within the meaning of 35 U.S.C. §101, §102, §103, or §112. Rather, these changes are primarily directed to form and are made simply for clarification.

II. REJECTIONS

The Office Action rejects claims 1, 3, 5, 14-16, and 26 under 35 USC § 102(e) as being anticipated by US Patent No. 5,890,222 to Agarwal et al. (hereinafter, "Agarwal"). Additionally, claims 2 and 4 stand rejected under 35 USC § 103(a) as being unpatentable over Agarwal in view of US Patent No. 7,023,744 to Shimanek et al. ("Shimanek"). Applicant respectfully traverses these rejections for at least the reasons present below.

As understood by Applicant, Agarwal relates to a data processing architecture that includes an instruction having an operation code field for storing an operation code and at least one operand field, where the operand field includes an indirect addressing mode indicator for indicating enablement of an indirect addressing mode. If an indirect addressing mode is enabled, a general purpose register address is selected from an address field in an indirect register. In a direct addressing mode (when the indirect addressing mode is not enabled), the data processing

unit addresses a selected one of the plurality of general purpose registers utilizing the general purpose register address during the execution of the operation code by the data processing unit.

As understood by Applicant, Shimanek relates to programmable logic devices with configuration memory cells that function both as RAM and ROM, where a PLD incorporating these memory cells to store configuration data can be mask-programmed with a customer design, rendering the PLD an application-specific integrated circuit (ASIC).

Claim 1, as amended herein, recites, *inter alia*:

> An operation-processing device for performing operation processing based on an arbitrary operation program, said device comprising:
>
> ***a register array*** having a plurality of registers each for holding an arbitrary value based on a write address and a write control signal and for ***outputting the held value to a signal line based on a read address***;
>
> ***an operation portion having an input coupled to said signal line independent of an intervening addressable register such that a value read from said register array to said signal line based on a read address is capable of being provided to said input without further addressing a register, the operation portion being operable for performing an operation on said value read from said register array to said signal line;***
>
> an instruction-decoding portion for decoding an operation instruction from an operation program for operating said operation portion, wherein said operation instruction includes at least one bit indicative of an access method; and
>
> an instruction-execution-controlling portion for controlling said register array and the operation portion in order to execute an operation instruction decoded by said instruction-decoding portion,
>
> ***wherein, in the event said at least one bit is indicative of a first access method, then said instruction-execution-controlling portion is operable for (i) selecting one of said registers of the register array based on said operation instruction, and (ii) based on a value held by said selected register, and without reference to a value previously loaded into another register, performing register-to-register addressing processing for selecting another of said registers of said register array; and***

> wherein, in the event said at least one bit is indicative of a second access method, then said instruction-execution-controlling portion is operable for selecting one of said registers based on said operation instruction, and not performing register-to-register addressing processing for selecting, based on a value held by said selected register, another of said registers of said register array. [Emphasis added.]

Applicant respectfully submits that Agarwal, even in view of Shimanek, does not teach or suggest the above combination of features recited in claim 1. More specifically, Agarwal does not teach or suggest, *inter alia*, "(i) selecting one of said registers of the register array based on said operation instruction, and (ii) based on a value held by said selected register, *and without reference to a value previously loaded into another register*, performing register-to-register addressing processing for selecting another of said registers of said register array." For instance, while Agarwal discusses indirect addressing based on instructions read from a register file (respective register files 236, which together form register array 238, in Fig. 31) coupled to a processing element (respective processing elements 230-234 in Fig. 3), Agarwal's instruction architecture requires preloading an indirect register (control registers 246 in Fig. 3; registers 330 and 350 in Figs. 5 and 6, respectively), and then selecting the indirect register based on an operand of a decoded instruction read from the register file and executed by the processing element. *See, e.g.,* Agarwal at col. 6, lines 50-57; col. 7, lines 24-34; col. 8, lines 31-35; FIGS. 3, and 5-7. As such, Agarwal's indirect addressing architecture stands in stark contrast to Applicant's claimed invention (claim 1) that implements indirect register-to-register addressing without referencing another register that must be preloaded (e.g., such preloading, for example, requiring additional cycles). Applicant further submits that Shimanek does not remedy the deficiencies in Agarwal discussed above with respect to Applicant's claim 1.

Accordingly, for at least the foregoing reasons, Applicant respectfully submits that claim 1 is patentable. Additionally, based at least on reasoning similar to that presented above with respect to claim 1, Applicant respectfully submits that claim 14 is also patentable.

III. DEPENDENT CLAIMS

Each of the other claims in this application is dependent on an independent claim discussed above, and is therefore believed patentable for at least the same reasons presented for the independent claim upon which it depends. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual reconsideration of the patentability of each on its own merits is respectfully requested.

CONCLUSION

In view of the above, it is submitted that all pending claims are patentable and the application is in condition for allowance, and Applicant respectfully requests early reconsideration and allowance of the application.

Applicant gratefully acknowledges the Examiner's consideration of this matter, and the Examiner is respectfully invited to contact Applicant's undersigned representative by telephone on any outstanding issue regarding the application.

Respectfully submitted,

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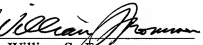
By 
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